LOW DIELECTRIC CONSTANT STI WITH SOI DEVICES

This application is a Divisional of U.S. Application No. 10/099,169 filed March 13, 2002, which is a Continuation-in-Part of U.S. patent application 09/503,278 filed on February 14, 2000, now U.S. Patent No. 6,413,827 issued July 2, 2002. These applications are incorporated herein by reference.

PAT 6,677,209

Technical Field

The present invention relates generally to isolation techniques in integrated circuits, and in particular to shallow trench isolation techniques having materials of low dielectric constant for use in the development and fabrication of integrated circuits.

Background

Implementing electronic circuits involves connecting isolated devices through specific electronic paths. In integrated circuit fabrication it is generally necessary to isolate adjacent devices from one another. They are subsequently interconnected to create the desired circuit configuration. In the continuing trend toward higher device densities, parasitic interdevice currents become more problematic, thus isolation technology has become a critical aspect of contemporary integrated circuit fabrication.

A variety of successful isolation technologies have been developed to address the requirements of different integrated circuit types such as NMOS, CMOS and bipolar. In general, the various isolation technologies exhibit different attributes with respect to such characteristics as minimum isolation spacing, surface planarity, process complexity and defect density generated during isolation processing. Moreover, it is common to trade off some of these characteristics when developing an isolation process for a particular integrated circuit application.